80115 Digitaalisuunnittelu, tentti 2.4.2001 (J. Niittylahti)

80115 Basic Digital Design, examination 2 April 2001

1. Implement a one-bit full adder
a) as a two-level gate network (NOT, AND, OR)
b) as a multi-level gate network with (NOT, XOR, NAND)
c) as a network using half-adder modules
d) as a ROM
e) with multiplexers

2. The circuit depicted in Fig. 1 is asynchronous. Redesign it to work in synchronous manner.

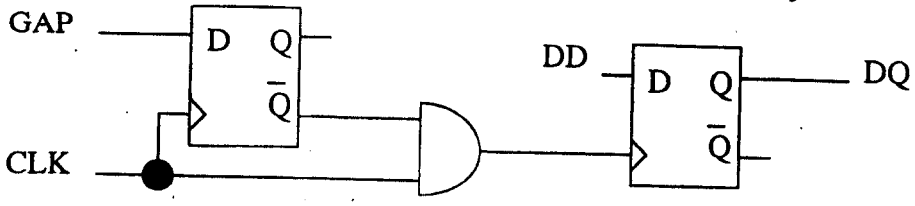

FIG. 1

3. Analyse the network depicted in Fig. 2. Give a state diagram of the sequential system.

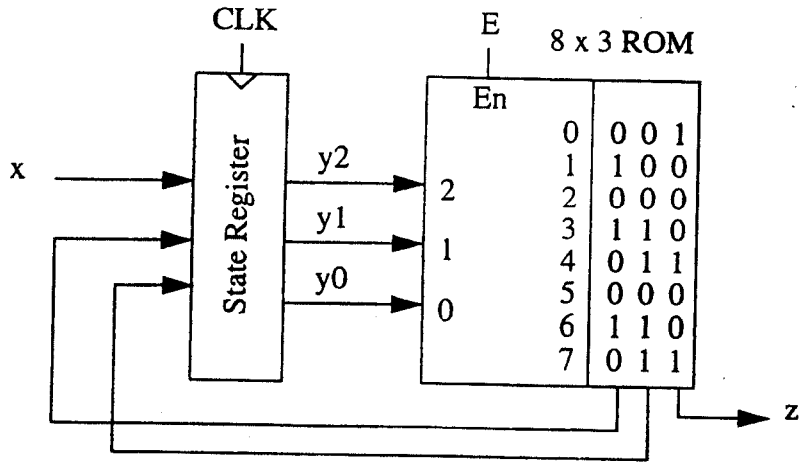

FIG. 2

4. Design a counter with the following counting sequence: 6, 7, 10, 11, 10, 11, 14, 15, 6, 7, ... Use a modulo-16 counter and logic gates.

5. Analyze the pattern recognizer of Fig. 3. Give a state diagram. Assuming that the initial state is 00, determine five input patterns that the system recognizes (produces a 1 output).

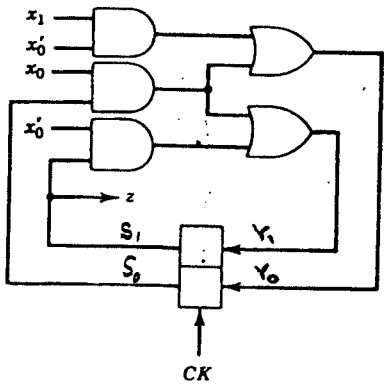

FIG. 3