80121 Prosessorien suunnittelu
Processor Design

tentti /exam
20.01.2001

1. A) Mitä ovat BDTImark ja DSPstone? Ottavatko ne huomioon kääntäjän vaikutuksen ja jos ottavat niin miten?

   What are BDTImark and DSPstone? Do they take into account the impact of the compiler and if they do, how?

   B) Mikä on käskykanta-arkkitehtuuri (Instruction Set Architecture, ISA)?

   What is Instruction Set Architecture (ISA)?

2. A) Kuvaa sovelluskohtaisen prosessorin suunnitteluvuo.

   Describe the design flow of an application-specific processor.

   B) Mikä on VLIW- ja superskalaariprosessorin ero?

   What is the difference between a VLIW and a superscalar processor?

3. Suunnittele 16-bittinen käskykoodaus seuraavan sivun taulukon mukaisille käskyille. Tavoitteena on mahdollisimman yhtenäinen koodaus kaikille käskyille. Vain yhden käskysanan käskyjä saa käyttää. Kommentoi!

   Design a 16-bit instruction coding for the instructions found in the table on next page. The target is to get the instruction coding as uniform as possible. Use only single-word instructions. Comment!

4. Suunnittele laitteistoarkkitehtuuri (mahdollisimman yksityiskohtainen lohkokaavio), jolla voi toteuttaa edellisen tehtävän käskyjen suorituksen.

   Design a hardware architecture (as detailed block diagram as possible) to implement the execution of the instructions of question 3.

5. Mitkä kolme pääosaa on signaaliprosessorissa? Luettele mahdollisimman kattavasti sen suunnitteluun vaikuttavia valintoja näissä eri osissa.

   What are the three main parts of a signal processor? Make a comprehensive list of design choices in these parts.

Table of instructions

General issues: 16 general purpose registers, 16-bit 2's complement data

INSTRUCTION	ADDRESSING MODES, LIMITATIONS, ETC.
Add	2 source and 1 destination registers
Add with carry	2 source and 1 destination registers
Subtract	2 source and 1 destination registers
Multiply	Mixture of signed and unsigned operands. 2 source and 1 **double** destination regs.
Logical shift	1 src, 1 dest reg, ±15 bit shifts from instruction
Logical shift on register	1 src, 1 dest reg, 1 shift-amount register
AND	2 source and 1 destination registers
OR	2 source and 1 destination registers
XOR	2 source and 1 destination registers
NOT	1 source and 1 destination registers
Conditional branch	Up to 7 conditions, PC-relative branch in ±255 range
Unconditional branch	PC-relative branch in ±255 range
Conditional branch on register	Up to 7 conditions, 1 reg. for branch address
Unconditional branch on register	1 reg. for branch address
Conditional branch and link on register	Up to 7 conditions, 1 reg. for branch address, 1 link register
Unconditional branch and link on register	1 reg. for branch address, 1 link register
Load	Register indirect with possible post-inc/dec, 1 dest reg.
Store	Register indirect with possible post-inc/dec, 1 src reg.
Load immediate	Signed ±127 immediate, 1 dest reg.
Register – register move	1 src and 1 dest reg.
No operation	